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PATENT APPLICATION

PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Tatsuya SHIMODA et al.

On Appeal from Group: 2815

Application No.: 09/892,872

Examiner: B. Baumeister

Filed: June 28, 2001

Docket No.: 109975

For: FERROELECTRIC MEMORY AND METHOD OF MAKING THE SAME

APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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For the convenience of the Finance Division, two additional copies of this transmittal letter are attached.

Respectfully submitted,

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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Tatsuya SHIMODA et al.	Group Art Unit: 2815
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BRIEF ON APPEAL

Appeal from Group 2815

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APPENDIX A A-1

I. INTRODUCTION

This is an appeal from an Office Action mailed March 4, 2004, finally rejecting claims 1-6, 8-10, 12-16 and 18-25 of the above-identified patent application.

A. Real Party in Interest

The real party in interest in this appeal in the present application is Seiko Epson Corporation, by way of an assignment recorded at reel/frame 12261/0941.

B. Statement of Related Appeals and Interferences

There are presently no appeals or interferences, known to Applicants, Applicants' representative or the Assignee, which will directly affect, be directly affected by or have a bearing on the Board's decision in the pending appeal.

C. Status of Claims

Claims 1-25 are pending. The outstanding Office Action withdrew claims 7, 11 and 17 from consideration. Claims 1-6, 8-10, 12-16 and 18-25 are on appeal. Of the claims that are on appeal, claims 1-3, 8-10, 12-14, 18 and 19 are independent claims. Claims 4-6 depend from claim 1. Claims 20 and 21 depend from claim 2. Claims 22 and 23 depend from claim 3. Claims 15 and 16 depend from claim 12. Claim 24 depends from claim 13. Claim 25 depends from claim 14. Claims 1-25 are set forth in the attached Appendix.

D. Status of Amendments

No Amendment After Final Rejection was filed. Rather, in view of the lengthy prosecution history of the present application, a Notice of Appeal was directly filed in response to the March 4, 2004 Final Rejection.

II. SUMMARY OF THE INVENTION AND APPLIED REFERENCES

A. Summary of the Invention

The invention is directed to various embodiments of ferroelectric memory and methods of fabricating a ferroelectric memory. See specification at paragraph [0012]. A

ferroelectric memory includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array. See specification at paragraphs [0003]-[0006]. The passive matrix array and the peripheral circuit are separately fabricated, integrated and electrically connected. See specification at paragraphs [0050] and [0065].

The invention also provides various methods of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array. See specification at paragraph [0056].

The invention variously provides for a passive matrix array and a peripheral circuit that are separately fabricated. See specification at paragraph [0043]. As a result of the separate fabrication of the passive matrix array and the peripheral circuit, the peripheral circuits are not adversely affected when fabricating the passive matrix array, thereby decreasing the degree of limitation in the fabrication process. See specification at paragraph [0043].

B. <u>The Claimed Invention</u>

The claimed invention is directed to various embodiments of ferroelectric memory and methods of fabricating a ferroelectric memory. See specification at paragraph [0012] and claims 1-25. A ferroelectric memory includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix

array, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array. See specification at paragraphs [0003] and [0004]; and claims 1-3, 8-10, 12-14, 18 and 19. The passive matrix array and the peripheral circuit are separately fabricated for integration and electrical connection of the passive matrix array with the peripheral circuit. See specification at paragraph [0042] and [0043]; and claims 1-3, 8-10, 12-14, 18 and 19. Certain other features of the various exemplary embodiments are briefly described below.

An exemplary embodiment of the invention provides a ferroelectric memory with a passive matrix array formed on a microstructure. See specification at paragraph [0014] and claim 1. The microstructure is centrally positioned and integrated on a substrate. See specification at paragraph [0056] and claim 1. A peripheral circuit is provided that includes at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array. See specification at paragraph [0058] and claim 1. The peripheral circuit is separately formed on the substrate. See specification at paragraph [0014] and claim 1. Other exemplary embodiments of the invention may include variations in the separate dispositions, such as the peripheral circuit being separately formed on a microstructure (specification at paragraph [0041] and claim 2); the passive matrix array being formed on a first microstructure and the peripheral circuit being separately formed on a second microstructure (specification at paragraph [0056] and claim 3); the passive matrix array, the peripheral circuit and the associated circuit being separately formed on the respective one of a plurality of microstructures (specification at paragraph [0017] and claim 8); the passive matrix array and the peripheral circuit being separately fabricated, positioned and integrated on a single microstructure (specification at paragraph [0022] and claim 9); and the passive matrix array being formed on a first microstructure, the first microstructure being provided in a central part of a second microstructure to be integrated (specification at paragraph [0023] and claim 10).

Other exemplary embodiments of the invention provide various methods of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array. See specification at paragraph [0025] and claims 12-14, 18 and 19. The passive matrix array and the peripheral circuit are separately fabricated. See specification at paragraph [0043] and claims 12-14, 18 and 19.

One exemplary method embodiment of the invention provides forming a passive matrix array on a microstructure, separately forming the peripheral circuit on a substrate, and centrally positioning and integrating the microstructure on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit. See specification at paragraph [0025] and claim 12. Other exemplary method embodiments of the invention may include variations in the separate formations, such as forming the passive matrix array centrally disposed on a substrate and separately forming a peripheral circuit on a microstructure (specification at paragraph [0026] and claim 13); forming a passive matrix array on a first microstructure and separately forming the peripheral circuit on a second microstructure (specification at paragraph [0027] and claim 14); forming a passive matrix array on a first microstructure and separately forming a peripheral circuit on a second microstructure which is larger than the first microstructure (specification at paragraph [0031] and claim 18);

Finally, another exemplary method embodiment of the invention provides separately forming a passive matrix array on each of a plurality of microstructures, and providing microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring. See specification at paragraph [0032] and claim 19.

C. The Rejection

The Final Rejection rejects claims 1-6, 8-10, 12-16 and 18-25 under 35 U.S.C. §103(a) over U.S. Patent No. 5,824,186 to Smith et al. (hereinafter, "Smith") in view of the Applicants' disclosure of related art (hereinafter, "Related Art"), and WO 99/12170 (hereinafter, "WO '170").

D. The Applied References

1. U.S. Patent No. 5,824,186 to Smith et al.

Smith discloses a method and apparatus for assembling microstructures onto a substrate through fluid transport. The microstructures are shaped blocks that are typically etched gallium arsenide blocks that self-align into recessed regions located on a substrate such that the microstructure becomes integral with the substrate (Abstract).

Smith does not teach or suggest that the etched gallium arsenide blocks may be separately processed to form "a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array," as recited in claims 1-3, 8-10, 12-14, 18 and 19. Rather, Smith merely discloses "such multi-layered structure may include metals, insulators such as silicon dioxide, silicon nitride, and the like, and the combinations thereof" (col. 4, lines 57-60).

2. WO 99/12170 PCT Application

WO '170 was disclosed in paragraph [0003] of the above-identified application. Paragraph [0003] discloses a conventional example of ferroelectric memory disclosed in International Patent Application No. WO99/12170 and Japanese Patent Application Laid Open No. 9-116107. A conventional ferroelectric memory includes a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged in rows and columns, and the peripheral circuits for performing data read or write operations for each memory cell.

As discussed in the Applicants' "Description of Related Art," such a conventional example of ferroelectric memory does not disclose or suggest a ferroelectric memory or a method of fabricating a ferroelectric memory, "wherein the passive matrix array and the peripheral circuits are separately fabricated," as variously claimed.

3. Applicants' Disclosure of Related Art

The present application discloses the related art, providing a conventional example of ferroelectric memory. Such a ferroelectric memory includes a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged in rows and columns, and peripheral circuits for performing data read or write operations for each memory cell and the like. See specification at paragraph [0003]. Such a conventional ferroelectric memory is fabricated by integrating the passive matrix array and the peripheral circuit on a single substrate in one plane. See specification at paragraph [0005].

The Applicants articulated the observed disadvantages of the conventional formation of the passive matrix array. For example, a high temperature treatment performed in an oxygen atmosphere for forming a ferroelectric film causes the preexisting MOS transistors on the same substrate to deteriorate. See specification at paragraph [0009].

The Applicants disclosed that in the case of integrating the passive matrix array and the peripheral circuits on a single substrate, such as in the case of fabricating a conventional ferroelectric memory, the fabrication process is limited to a large extent as described. See specification at paragraph [0011].

III. THE ISSUE ON APPEAL

1. Whether claims 1-6, 8-10, 12-16 and 18-25 are properly rejected under 35 U.S.C. §103(a) over Smith in view of the Applicants' specification disclosure of Related Art at paragraphs 3-11 and WO 99/12170.

IV. GROUPING THE CLAIMS ON APPEAL

Each claim of this patent application on appeal is separately patentable, and upon issuance of a patent will be entitled to a separate presumption of validity under 35 U.S.C. §282. For convenience in the handling of this appeal, the claims are grouped as follows:

Group I, claims 1-6, 8-10 and 20-23.

Group II, claims 12-16, 18, 24 and 25.

Group III, claim 19.

Each of Groups I-III are argued separately in the following arguments. The groups do not stand or fall together.

V. ARGUMENTS

A. Law on Obviousness under 35 U.S.C. §103(a)

In rejecting claims under 35 U.S.C. 103, it is incumbent on the examiner to establish a factual basis to support the legal conclusion of obviousness. See, In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), including: (A) determining the scope and content of the prior art; (B) ascertaining the differences between the prior art and the claims in issue; (C) resolving the level of ordinary skill in the pertinent art; and (D) evaluating evidence of secondary considerations. The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-84 (Fed. Cir. 1992).

In applying 35 U.S.C. §103(a), the Patent Office must: (A) consider the claimed invention as a whole; (B) consider the references as a whole when determining whether the references suggest the desirability of making a combination; (C) consider the references

without the benefit of impermissible hindsight consideration of Applicant's disclosure; and (D) use a reasonable standard of success as the standard from which obviousness is determined. Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1143, 229 USPQ 182, 187 (Fed. Cir. 1986).

In this regard, prior art must be viewed prospectively and not retrospectively using the patent as a blueprint to reconstruct the invention by indiscriminately picking and choosing parts and bits from the prior art. See, for example, Grain Processing Corp. v. American Maize-Products Co., 840 F.2d 902, 907, 5 USPQ2d 1788, 1792 (Fed. Cir. 1988) ("Care must be taken to avoid hindsight reconstruction by using 'the patent in suit as a guide through the maze of prior art references, combining the right references in the right way so as to achieve the result of the claims in suit.' "). See also In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention."). This is because "[t]o imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." W. L. Gore Associates Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), *cert. Denied*, 469 U.S. 851 (1984).

B. Claims 1-6, 8-10 and 20-23 are Not Obvious over Smith in View of the Applicants' Related Art Disclosure and WO 99/12170

Claims 1-6, 8-10 and 20-23 stand finally rejected under 35 U.S.C. §103(a) over Smith in view of the Applicants' specification disclosure of Related Art at paragraphs 3-11 and WO '170.

Independent claim 1 recites, *inter alia*, " A ferroelectric memory, comprising: ... a passive matrix array that includes memory cells formed of ferroelectric capacitors, ... the

passive matrix array being formed on the microstructure; ... a substrate, the microstructure being centrally positioned and integrated on the substrate; and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit, and wherein the passive matrix array and the peripheral circuit are separately fabricated."

Examiner asserts that WO '170 furnishes the ferroelectric capacitor disclosure (March 4, 2004 Final Rejection at paragraph 2), Smith teaches microstructures on a substrate and Applicants disclose the drawback of conventional formation of the passive matrix array, and are applied in combination (August 19, 2003 Office Action at paragraph 2).

As the Examiner admits, "Smith does not teach that ferroelectric-capacitor passive matrix arrays and/or associated peripheral circuits, specifically, may be employed with the Smith microstructure-on-substrate invention" (August 19, 2003 Office Action at page 3). However the Examiner asserts that "it was known that this integration poses the drawback of less than optimal device performance (paragraphs [0009]-[0011])" (August 19, 2003 Office Action at page 3). This assertion is respectfully traversed.

The disclosure of Related Art fails to overcome the deficiencies of Smith. Paragraphs [0009] - [0011] disclose the Applicants' observed problems with the conventional formation of the passive matrix array. These disadvantages of the conventional formation of passive matrix array were observed by Applicants. Applicants' comments regarding the disadvantages of the conventional formation of passive matrix array are not themselves prior art. Accordingly, the disclosed paragraphs [0009] - [0011] do not cure the deficiencies of Smith. The mere fact that the prior art may be modified in the manner suggested by the examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783-

84 (Fed. Cir. 1992). "To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher." W. L. Gore Associates Inc. v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983), *cert. Denied*, 469 U.S. 851 (1984).

WO '170 also fails to cure the deficiencies of Smith. As discussed in Applicants' November 14, 2003, Amendment, WO '170 merely describes a conventional ferroelectric data processing device with a ferroelectric thin film provided between a first and a second electrode structure, but does not teach, suggest or provide motivation for the passive matrix array being separately formed from the peripheral circuit. Accordingly, WO '170 also does not cure the deficiencies of Smith.

The Examiner further asserts that "it must be recognized that any judgment unobviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleamed only from the Applicants' disclosure, such a reconstruction is proper" (August 19, 2003 Office Action at paragraph 4. Applicants respectfully disagree with the Examiner's ultimate conclusions regarding claims 1-6, 8-10 and 20-23.

Any suggestion or motivation for deriving the recited claimed features can only be derived from the knowledge gleamed from the Applicants' disclosure, and cannot be knowledge which was within the level of ordinary skill at the time the claimed invention was made. As set forth above, Smith, disclosure of Related Art and WO '170 do not teach, suggest or provide prior-art motivation to derive any such features to even infer the specific features of claim 1 as recited. See In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600

(Fed. Cir. 1988) ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

For at least the reasons set forth above for claim 1, and for the specific features recited in claims 2, 3 and 8-10, Applicants respectfully disagree with the Examiner's ultimate conclusions regarding claims 2, 3 and 8-10. Smith, Applicants' disclosed related art and WO '170 also fail to teach or suggest the ferroelectric memory at claims 2, 3 and 8-10.

Accordingly, independent claims 1-3 and 8-10 are not obvious over Smith, either alone or in combination with related art and WO '170. The applied references also fail to render obvious the subject matter of dependent claims 4-6, which depend from claim 1; 20 and 21, which depend from claim 2; and claims 22 and 23, which depend from 3, and are allowable at least for their dependence thereon and for the additional features recited therein.

Reversal of the rejection of claims 1-6, 8-10, 12, 15, 16 and 20-23 under 35 U.S.C. §103(a) is therefore respectfully solicited.

C. Claims 12-16, 18, 24 and 25 are Not Obvious over Smith in View of the Applicants' Related Art Disclosure and WO 99/12170

Claims 12-16, 18, 24 and 25 stand finally rejected under 35 U.S.C. §103(a) over Smith in view of the Applicants' specification disclosure of Related Art at paragraphs 3-11 and WO '170.

Independent claim 12 recites, *inter alia*, "A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, ... and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the method comprising: forming the passive matrix array on a microstructure; separately forming the peripheral circuit on a substrate; and centrally positioning and integrating the microstructure on the substrate,

wherein the passive matrix array is electrically connected to the peripheral circuit; and wherein the passive matrix array and the peripheral circuit are separately fabricated."

Examiner asserts that WO '170 furnishes the ferroelectric capacitor disclosure (March 4, 2004 Final Rejection at paragraph 2), Smith teaches etching microstructures for assembly into matching recessed regions and Applicants disclose the drawback of conventional formation of the passive matrix array, and are applied in combination (August 19, 2003 Office Action at paragraph 2).

As previously set forth and admitted by the Examiner, Smith does not teach or suggest "the passive matrix array is electrically connected to the peripheral circuit; and wherein the passive matrix array and the peripheral circuit are separately fabricated" as recited in claims 1-3, 8-10 and 12. The Examiner specifically states that "Smith does not teach that ferroelectric-capacitor passive matrix arrays and/or associated peripheral circuits, specifically, may be employed with the Smith microstructure-on-substrate invention" (August 19, 2003 Office Action at page 3).

The disclosed Related Art fails to overcome the deficiencies of Smith. As discussed above, the Applicants' comments regarding the disadvantages of the conventional formation of the passive matrix array are not themselves prior art, and therefore do not provide the prior-art motivation for combining or modifying references. Accordingly, the disclosed Related Art does not cure the deficiencies of Smith.

WO '170 also fails to cure the deficiencies of Smith. As previously set forth, WO '170 merely describes a conventional ferroelectric data processing device with a ferroelectric thin film provided between a first and a second electrode structure, but does not teach, suggest or provide prior-art motivation for "forming the passive matrix array on a microstructure; separately forming the peripheral circuit on a substrate; and centrally positioning and

integrating the microstructure on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit," as recited in claim 12.

Even if combined, Smith, the disclosed Related Art and WO '170 do not result in a method of fabricating a ferroelectric memory in which a passive matrix array is formed on a microstructure and a peripheral circuit is separately formed on a substrate, the microstructure being centrally positioned and integrated onto the substrate, as recited in claim 12. As previously set forth, the Applicants' comments regarding the disadvantages of the conventional formation of the passive matrix array are not themselves prior art, and therefore do not provide the prior-art motivation for combining or modifying references. Accordingly, the disclosed Related Art does not cure the deficiencies of Smith.

For at least the reasons set forth above for claim 12, and for the specific features recited in claims 13, 14 and 18, Applicants respectfully disagree with the Examiner's ultimate conclusions regarding claims 13, 14 and 18. Smith, Applicants' disclosed related art and WO '170 also do not teach or suggest the methods of claims 13, 14 and 15.

Accordingly, independent claims 12-14 and 18 are not obvious over Smith, either alone or in combination with the disclosed Related Art and WO '170. The applied references also fail to render obvious the subject matter of dependent claims 15 and 16, which depend from base claim 12; claim 24, which depends from claim 13; and claim 25, which depends from claim 14, and are allowable at least for their dependence thereon and for the additional features recited therein.

Reversal of the rejection of claims 12-16, 18, 24 and 25 under 35 U.S.C. §103(a) is therefore respectfully solicited.

D. Claim 19 is Not Obvious over Smith in View of the Applicants' Related Art Disclosure and WO 99/12170

Claim 19 stands finally rejected under 35 U.S.C. §103(a) over Smith in view of the Applicants' specification disclosure of Related Art at paragraphs 3-11 and WO '170.

Independent claim 19 recites, *inter alia*, "A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, ... and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising: separately forming the passive matrix array on each of a plurality of microstructures; and providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring."

The Examiner failed to address the specific features of "providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring," as recited in claim 19. Such shortcomings of the Office Action's response were succinctly pointed out to Examiner Baumeister by the Applicants' representative in the December 3, 2003, personal interview for Examiner's further consideration.

Furthermore, Smith, the disclosed Related Art and WO '170 do not combine to result in a method of fabricating a ferroelectric memory in which the passive matrix array is separately formed on each of a plurality of microstructures, the microstructures being provided in layers to be integrated in a substrate, as recited in claim 19. As previously set forth, the Applicants' comments regarding the disadvantages of the conventional formation of the passive matrix array are not themselves prior art, and therefore do not provide the prior-art motivation for combining or modifying references. Accordingly, the disclosed Related Art does not cure the deficiencies of Smith.

For at least these reasons, and for the reasons previously set forth, Applicants respectfully disagree with the Examiner's ultimate conclusions regarding claim 19. Smith, Applicants' disclosed Related Art and WO '170 do not teach or suggest the method of fabricating a ferroelectric memory of claim 19.

Accordingly, independent claim 19 is not obvious from Smith, either alone or in combination with the disclosed Related Art and WO '170. Reversal of the rejection with respect to claim 19 under 35 U.S.C. §103(a) is therefore respectfully solicited.

VI. Conclusion

For at least the reasons discussed above, it is respectfully submitted that at least claims 1-6, 8-10, 12-16 and 18-25 contain patentable subject matter and are distinguishable over the applied references.

Applicant respectfully requests the Honorable Board to reverse the final rejection of the claims and return the application to the Examiner to pass this case to issue.

Respectfully submitted,

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Enclosure:
Appendix of Claims

APPENDIX A

CLAIMS:

1. A ferroelectric memory, comprising:

a microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the microstructure;

a substrate, the microstructure being centrally positioned and integrated on the substrate; and

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the peripheral circuit being separately formed on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

2. A ferroelectric memory, comprising:

a substrate;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the substrate;

a microstructure; and

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the peripheral circuit being separately formed on the microstructure, the microstructure being peripherally positioned and integrated

on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

3. A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the first microstructure;

a second microstructure;

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the peripheral circuit being separately formed on the second microstructure; and

a substrate, the first and second microstructures being integrated on the substrate, wherein the peripheral circuit is peripherally positioned and electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

4. The ferroelectric memory according to claim 1, further including a plurality of microstructures integrated on the substrate, the passive matrix array being formed on each of the plurality of microstructures.

5. The ferroelectric memory according to claim 1, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

6. The ferroelectric memory according to claim 5,

wherein the substrate is formed by transfer-molding a photocurable resin.

7. A ferroelectric memory, comprising:

a first microstructure;

a plurality of pairs of a passive matrix array that each includes memory cells formed of ferroelectric capacitors, the plurality of pairs of the passive matrix array being provided on the first microstructure;

a second microstructure;

a peripheral circuit for the passive matrix array, the peripheral circuit being formed on the second microstructure; and

a substrate, at least one of the pairs of the passive matrix array being provided on each side of the substrate.

8. A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array,

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array;

an associated circuit having a same or a different function as the memory cells;

a single substrate; and

a plurality of microstructures, the passive matrix array, the peripheral circuit and the associated circuit being separately formed on each of the plurality of microstructures, the microstructures being integrated on the single substrate, wherein the peripheral circuit is positioned and electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

9. A ferroelectric memory, comprising:

a passive matrix array that includes memory cells formed of ferroelectric capacitor, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array,

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array; and

a single microstructure, the passive matrix array and the peripheral circuit being separately fabricated, positioned and integrated on the single microstructure, wherein the peripheral circuit is peripherally positioned and electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

10. A ferroelectric memory, comprising:

a first microstructure;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, the passive matrix array being formed on the first microstructure;

a second microstructure that is larger than the first microstructure, the first microstructure being provided in a central part of the second microstructure to be integrated; and

a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the peripheral circuit being separately formed on the second microstructure, wherein the peripheral circuit is electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

11. A ferroelectric memory, comprising:

a plurality of microstructures;

a passive matrix array that includes memory cells formed of ferroelectric capacitors, the passive matrix array being formed on each of the plurality of microstructures;

a peripheral circuit for the passive matrix array; and

a substrate, the microstructures being provided in layers to be integrated in the substrate.

12. A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the method comprising:

forming the passive matrix array on a microstructure;

separately forming the peripheral circuit on a substrate; and

centrally positioning and integrating the microstructure on the substrate, wherein the passive matrix array is electrically connected to the peripheral circuit; and wherein the passive matrix array and the peripheral circuit are separately fabricated

13. A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the method comprising:

forming the passive matrix array centrally disposed on a substrate;

separately forming the peripheral circuit on a microstructure; and

integrating the microstructure on the substrate, wherein the peripheral circuit is peripherally positioned and electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

14. A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure; and

integrating the first and second microstructures on a substrate, wherein the peripheral circuit is peripherally positioned and electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

15. The method of fabricating a ferroelectric memory according to claim 12, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

16. The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the step of providing the microstructure includes providing a fluid which contains the microstructure to a surface of the substrate.

17. A method of fabricating a ferroelectric memory which includes a passive matrix array including memory cells formed of ferroelectric capacitors, and a peripheral circuit for the passive matrix array, the method comprising:

forming a plurality of pairs of the passive matrix array on a first microstructure;

forming the peripheral circuit on a second microstructure; and

integrating at least one of the pairs on each side of a substrate.

18. A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit including at least a word line driver circuit and a bit line driver circuit for driving the passive matrix array, the method comprising:

forming the passive matrix array on a first microstructure;

separately forming the peripheral circuit on a second microstructure which is larger than the first microstructure; and

providing the first microstructure in a central part of the second microstructure to be integrated, wherein the peripheral circuit is electrically connected with the passive matrix array, and wherein the passive matrix array and the peripheral circuit are separately fabricated.

19. A method of fabricating a ferroelectric memory, which includes a passive matrix array including memory cells formed of ferroelectric capacitors, a ferroelectric capacitor being defined by an intersection of row and column electrodes sandwiching a ferroelectric film common to the passive matrix array, and a peripheral circuit comprising a line driver circuit peripheral to the passive matrix array, the method comprising:

separately forming the passive matrix array on each of a plurality of microstructures; and

providing the microstructures in layers to be integrated in a substrate, wherein the passive matrix array on each of the plurality of microstructures is electrically connected to a respective drain wiring.

20. The ferroelectric memory according to claim 2, further including a plurality of microstructures integrated on the substrate, at least one of word line driver circuit and bit line driver circuit being formed on each of the plurality of microstructures.

21. The ferroelectric memory according to claim 2, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

22. The ferroelectric memory according to claim 3, further including a plurality of microstructures integrated on the substrate, the passive matrix array and at least one of word line driver circuit and bit line driver circuit being formed on each of the plurality of microstructures.

23. The ferroelectric memory according to claim 3, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

24. The method of fabricating a ferroelectric memory according to claim 13, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.

25. The method of fabricating a ferroelectric memory according to claim 14, further including:

forming a recess portion in the substrate which corresponds to a shape of the microstructure; and

providing the microstructure in the corresponding recess portion in the substrate to be integrated.